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EXAMINER	
STEVENSON, ANDRE C	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,324	PARIKH ET AL.	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *27-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Information Disclosure Statement

The information disclosure statement (IDS) submitted on July 02, 2004 was before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Election/Restrictions

Applicant's election without traverse of Group I, claims #1-26 in the reply filed on October 10, 2005 is acknowledged.

Claims 27-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 10, 2005.

Claim Objections

Claims #5, 6, 18 and 19 are objected to because of the following informalities: Claims #5 and 6 are duplicates of each other. Also, claims #18 and 19 are duplicates of each other. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims #1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. (U.S. Pub. 2005.0084987 A1, Pub. Date 04/21/05, Filed 10/20/04, PCT File Date 04/13/00), and in view of Somekh et al. (U.S. Pat. No.6,640,151 B1, Patented 10/28/03, Filed 12/22/99).

Wilson substantially shows the claimed invention, as shown in figures #1-7 and corresponding text, **pertaining to claim #1**, a method generating, in response to deposition results, first control parameters; performing electrochemical plating to deposit a copper layer upon the barrier and seed layer **(page #14, paragraph 0120-0122; page #8, paragraph 0069)**; generating, in response to plating results, second control parameters; polishing upon the copper layer; generating, in response to polishing results, third control parameters; and controlling at least one of the polishing process in response to the first control parameters or the deposition process in response to the third control parameters **(page #3, paragraph 0024).** Examiner notes that the preamble of claim #1 has not been given any patentable weight. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). ***Pertaining to claim #3,*** Wilson shows, a method wherein a step of controlling a polishing process comprises: controlling at least one of control radial pressure profile and the rotational speed of the polishing pad in response to at least one of the 'first, second or third control parameters **(page #3, paragraph 0024)**. ***Pertaining to claim #5,*** Wilson shows, a method wherein the step of controlling the depositing process further comprises: controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters **(page #4, paragraph 0038).** ***Pertaining to claim #6,*** Wilson shows, a method wherein the step of controlling the depositing process further

comprises: controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters **(page #4, paragraph 0038).** ***Pertaining to claim #7,*** Wilson shows, a method of claim 1, wherein the step of controlling the plating process further comprises: controlling at least one of electroless thickness, patch thickness, current or pulse sequence, or additives to compensate for at least one of voids or planarization issues **(page #4 & 5, paragraph 0040).** ***Pertaining to claim #10,*** Wilson teaches a method wherein the step of tuning plating parameters further comprises: controlling at least one of current density, rotation speed, and anode to wafer distance in response to the gap fill information **(page #13, paragraph 0116).** ***Pertaining to claim #11,*** Wilson teaches a method further comprising: tuning polishing parameters of the wafer in response to the gap fill information **(page #3, paragraph 0024).** ***Pertaining to claim #12,*** Wilson teaches a method further comprising: tuning processing parameters of subsequently process wafers in response to the control parameters **(page #3, paragraph 0024). Pertaining to claim #13,** Wilson shows, a method wherein at least one of the results utilized to generate the control parameters are selected from the group consisting of barrier seed step coverage of a trench and via having a specific size aspect ratio, gap fill, void detection, planarization, dishing, erosion, copper thickness, trench depth, dielectric constant, residual metal on a comb structure, via or snake open in a standard structure based on a voltage contrast or two-probe measurement, barrier thickness, copper seed thickness, copper thickness, copper bulk resistance, dielectric thickness, dielectric constant, presence of particles, presence of residue and systematic process defects **(page #9, paragraph 0080 and 0082; page #4, paragraph 0033).** ***Pertaining to claim #14,*** Wilson shows, a method of testing a barrier and seed layer thickness; generating, in

response to the barrier and seed layer thickness, first control parameters for the electrochemical plating tool and the barrier and seed layer deposition tool **(page #14, paragraph 0128; page #4, paragraph 0037)** performing electrochemical plating to deposit a copper layer upon the barrier and seed layer in accordance with the control parameters **(page #3, paragraph 0020)**; testing at least one of copper thickness and resistively **(page #6, paragraph 0051)**; generating, in response to the testing at least ones of copper thickness and resistively **(page #6, paragraph 0051)**, second control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool **(page #3, paragraph 0024)**, and the chemical-mechanical polishing tool; performing chemical-mechanical polishing upon the copper layer in accordance with the second control parameters **(page #3, paragraph 0024).** Examiner notes that the preamble of claim #14 has not been given any patentable weight. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). ***Pertaining to claim #18,*** Wilson shows, a method wherein the step of controlling the deposition tool further comprises: controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters **(page #2, paragraph 0018).** ***Pertaining to claim #19,*** Wilson shows, a method wherein the step of controlling the deposition tool further comprises: controlling at least one of power, pressure, bias, time of gas flows to change deposition thickness in response to at least one of the first, second or third control parameters **(page #2, paragraph 0018).** ***Pertaining to claim #20,*** Wilson shows, a method wherein the step of controlling the electrochemical plating tool further comprises: controlling at least one of electroless thickness, patch thickness, current or pulse sequence, or additives to compensate for at least one of voids or planarization issues **(page #7,**

paragraph 0057). ***Pertaining to claim #23,*** Wilson shows, a method wherein the step of tuning plating parameters further comprises: controlling at least one of current density, rotation speed, and anode to wafer distance in response to the gap fill information **(page #13, paragraph 0116).** ***Pertaining to claim #24,*** Wilson shows a method further comprising: tuning polishing parameters of the wafer in response to the gap fill information **(page #3, paragraph 0024).** ***Pertaining to claim #25,*** Wilson shows, a method of generating, in response to deposition results, first control parameters; performing electrochemical plating to deposit a copper layer upon the barrier and seed layer; polishing upon the copper layer; and controlling the polishing process in response to the first control parameters **(page #3, paragraph 0024; page #8, paragraph 0069; page #14, paragraph 0120-0122). Pertaining to claim #26,** Wilson shows, a method of performing electrochemical plating to deposit a copper layer upon the barrier and seed layer; polishing upon the copper layer; generating, in response to polishing results, first control parameters; and controlling the deposition process in response to the first control parameters **(page #3, paragraph 0024; page #8, paragraph 0069; page #14, paragraph 0120-0122).**

Wilson fails to show, with respect to **claim #1**, a method of depositing a barrier and seed layer within a trench formed in the semiconductor wafer.

Wilson fails to show, with respect to **claim #2**, a method further comprising: etching the trench into the semiconductor wafer; testing a trench geometry; generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and using the fourth control parameters to process the semiconductor wafer having the trench geometry.

Wilson fails to show, with respect to **claim #4**, a method wherein the step of controlling the polishing process further comprises: setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first, second or third control parameters.

Wilson fails to show, with respect to **claim #8**, a method further comprising: obtaining gap fill information.

Wilson fails to show, with respect to **claim #9,** a method further comprising: tuning plating parameters of subsequently plated wafers in response to the gap fill information.

Wilson fails to show, with respect to **claim #14,** a method of depositing a barrier and seed layer within a trench formed in the semiconductor wafer, testing a copper uniformity and residue of the polished semiconductor wafer; generating, in response to the copper uniformity and residue, third control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; using the third control parameters in processing subsequent semiconductor wafers.

Wilson fails to show, with respect to **claim #15,** a method further comprising: etching the trench into the semiconductor wafer; testing a trench geometry; generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and using the fourth control parameters to process the semiconductor wafer having the trench geometry.

Wilson fails to show, with respect to **claim #16,** a method wherein the step of controlling the chemical mechanical polishing tool further comprises: setting at least one of control radial

pressure profile and the rotational speed of the polishing pad in response to at least one of the second or third control parameters.

Wilson fails to show, with respect to **claim #17,** a method wherein the step of controlling the chemical mechanical polishing tool further comprises: setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first or third control parameters.

Wilson fails to show, with respect to **claim #21,** a method further comprising: obtaining gap fill information

Wilson fails to show, with respect to **claim #22,** a method further comprising: tuning plating parameters of subsequently plated wafers in response to the gap fill information.

Wilson fails to show, with respect to **claim #25,** a method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising: depositing a barrier and seed layer within a trench formed in the semiconductor wafer.

Wilson fails to show, with respect to **claim #26,** a method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising: depositing a barrier and seed layer within a trench formed in the semiconductor wafer.

Somekh teaches, in a similar method for a multi tool controlling system, with respect to **claim #1**, a method of depositing a barrier and seed layer within a trench formed in the semiconductor wafer **(column 6, lines 23-65)**. ***Pertaining to claim #2,*** Somekh teaches, a method further comprising: etching the trench into the semiconductor wafer; testing a trench geometry; generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and using the fourth control parameters to process the semiconductor wafer having the trench geometry **(column 6, lines 23-65)**. ***Pertaining to claim #4,*** Somekh teaches a method wherein the step of controlling the polishing process further comprises: setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first, second or third control parameters **(column 11, lines 14-37)**. ***Pertaining to claim #8,*** Somekh teaches a method further comprising: obtaining gap fill information **(column 6, lines 23-65)**. ***Pertaining to claim #9,*** Somekh teaches a method further comprising: tuning plating parameters of subsequently plated wafers in response to the gap fill information **(column 6, lines 23-65)**. ***Pertaining to claim #14,*** Somekh teaches a method of depositing a barrier and seed layer within a trench formed in the semiconductor wafer **(column 6, lines 23-65)**, testing a copper uniformity and residue of the polished semiconductor wafer; generating, in response to the copper uniformity and residue, third control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; using the third control parameters in processing subsequent semiconductor wafers **(column 6, lines 23-65)**. ***Pertaining to claim #15,*** Somekh teaches a method further comprising: etching the trench into the semiconductor wafer;

testing a trench geometry; generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and using the fourth control parameters to process the semiconductor wafer having the trench geometry **(column 6, lines 23-65)**. ***Pertaining to claim #16,*** Somekh teaches a method wherein the step of controlling the chemical mechanical polishing tool further comprises: setting at least one of control radial pressure profile and the rotational speed of the polishing pad in response to at least one of the second or third control parameters **(column 11, lines 14-37)**. ***Pertaining to claim #17,*** Somekh teaches a method wherein the step of controlling the chemical mechanical polishing tool further comprises: setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first or third control parameters **(column 11, lines 14-37)**. ***Pertaining to claim #21,*** Somekh teaches a method further comprising: obtaining gap fill information **(column 6, lines 23-65)**. ***Pertaining to claim #22,*** Somekh teaches a method of claim 21 further comprising: tuning plating parameters of subsequently plated wafers in response to the gap fill information **(column 6, lines 23-65)**. ***Pertaining to claim #25,*** Somekh teaches a method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising: depositing a barrier and seed layer within a trench formed in the semiconductor wafer **(column 6, lines 23-65)**. ***Pertaining to claim #26,*** Somekh teaches a method of monitoring and controlling copper interconnect manufacturing processes within a multi-step

copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising: depositing a barrier and seed layer within a trench formed in the semiconductor wafer **(column 6, lines 23-65)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #1**, a method of depositing a barrier and seed layer within a trench formed in the semiconductor wafer, into the method of Wilson, as taught by Somekh, with the motivation that depositing a seed and barrier layer within the trench is needed to initiate copper electrochemical deposition (ECD). It is well known in the art to that the use of an ECD process to deposit copper within a narrow area, precludes copper from being deposited on the sidewalls of the trench.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #2**, to include a method further comprising: etching the trench into the semiconductor wafer; testing a trench geometry; generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and using the fourth control parameters to process the semiconductor wafer having the trench geometry, , into the method of Wilson, as taught by Somekh, with the motivation that the implementation of the procedures listed above provides a facility to query one or more tools/products to determine whether or not the tools/products are ready for the production of a specified semiconductor

product and/or for the implementation of required/requested steps so that appropriate actions can be taken.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #4**, to include a method wherein the step of controlling the polishing process further comprises: setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first, second or third control parameters, into the method of Wilson, as taught by Somekh, with the motivation that controlling the polishing process provides a means for modification to a recipe to increase the quality of the product without effecting the entire recipe.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #8**, to include a method further comprising: obtaining gap fill information, into the method of Wilson, as taught by Somekh, with the motivation that this provides a system method and medium information, for facilitating communications among the tools in the semiconductor processing facility.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #9**, to include a method further comprising: tuning plating parameters of subsequently plated wafers in response to the gap fill information, into the method of Wilson, as taught by Somekh, with the motivation that controlling the plating process provides a means for modification to a recipe, to increase the quality of the product without effecting the entire recipe.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #14**, to include a method of depositing a barrier and

seed layer within a trench formed in the semiconductor wafer, testing a copper uniformity and residue of the polished semiconductor wafer; generating, in response to the copper uniformity and residue, third control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; using the third control parameters in processing subsequent semiconductor wafers, into the method of Wilson, as taught by Somekh, with the motivation that depositing a seed and barrier layer within the trench is needed to initiate copper electrochemical deposition (ECD). It is well known in the art to that the use of an ECD process to deposit copper within a narrow area, precludes copper from being deposited on the sidewalls of the trench. Also, implementation of the procedures listed above, provides a facility to query one or more tools/products to determine whether or not the tools/products are ready for the production of a specified semiconductor product and/or for the implementation of required/requested steps so that appropriate actions can be taken.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #15**, to include a method further comprising: etching the trench into the semiconductor wafer; testing a trench geometry; generating, in response to the trench geometry, fourth control parameters for the electrochemical plating tool, the barrier and seed layer deposition tool, and the chemical-mechanical polishing tool; and using the fourth control parameters to process the semiconductor wafer having the trench geometry, into the method of Wilson, as taught by Somekh, with the motivation that the implementation of the procedures listed above provides a facility to query one or more tools/products to determine whether or not the tools/products are ready for the production of a specified semiconductor

product and/or for the implementation of required/requested steps so that appropriate actions can be taken.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #16**, to include a method wherein the step of controlling the chemical mechanical polishing tool further comprises: setting at least one of control radial pressure profile and the rotational speed of the polishing pad in response to at least one of the second or third control parameters, into the method of Wilson, as taught by Somekh, with the motivation that controlling the CMP tool provides the option of preferentially removing material from the thick region , thereby improving the planarity of the resulting wafer and compensating fro variations in a prior tool.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #17**, to include a method wherein the step of controlling the chemical mechanical polishing tool further comprises: setting at least one of total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing in response to at least one of the first or third control parameters, into the method of Wilson, as taught by Somekh, with the motivation that controlling the CMP tool provides the option of preferentially removing material from the thick region , thereby improving the planarity of the resulting wafer and compensating fro variations in a prior tool.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #21**, to include a method further comprising of obtaining gap fill information, into the method of Wilson, as taught by Somekh, with the

motivation that this provides a system method and medium information, for facilitating communications among the tools in the semiconductor processing facility.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #22**, to include a method further comprising: tuning plating parameters of subsequently plated wafers in response to the gap fill information, into the method of Wilson, as taught by Somekh, with the motivation that controlling the plating process provides a means for modification to a recipe, to increase the quality of the product without effecting the entire recipe.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #25**, to include a method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising: depositing a barrier and seed layer within a trench formed in the semiconductor wafer, into the method of Wilson, as taught by Somekh, with the motivation that the implementation of the procedures listed above provides a facility to query one or more tools to determine whether or not the tools are ready for the production of a specified semiconductor product and/or for the implementation of required/requested steps so that appropriate actions can be taken.

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to **claim #26**, to include a method of monitoring and controlling copper interconnect manufacturing processes within a multi-step copper interconnect

manufacturing system having independently operating tools that perform specific processes upon a semiconductor wafer, wherein the tools include a barrier and seed layer deposition tool, a electrochemical plating tool and a chemical-mechanical polishing tool, comprising: depositing a barrier and seed layer within a trench formed in the semiconductor wafer, into the method of Wilson, as taught by Somekh, with the motivation that the implementation of the procedures listed above provides a facility to query one or more tools to determine whether or not the tools are ready for the production of a specified semiconductor product and/or for the implementation of required/requested steps so that appropriate actions can be taken.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosureIacoponi et al. (U.S. Pat. No. 6,489,240), Cohen (U.S. Pat. No. 6,903,016), Etherington (U.S. Pat. No. 6,231,743), Pasadyn et al. (U.S. Pat. No. 6,444,481), Cohen (U.S. Pat. No. 6,610,151), Woo et al. (U.S. Pat. No. 6,228,768), Kocimishki (U.S. Pat. No. 6,816,806), Liu et al. (U.S. Pat. No. 6,225,223), Liu et al. (U.S. Pat. No. 6,010,962), Sonderman et al. (U.S. Pub. No. 2002/0192944 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

10/24/05